(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 550 770 A1**

(12) **EUROPEAN PATENT APPLICATION published in accordance with Art. 158(3) EPC**

(21) Application number: **92916224.6**

(51) Int. Cl.5: **H01L 29/784**

(22) Date of filing: **22.07.92**

(86) International application number: **PCT/JP92/00929**

(87) International publication number: **WO 93/03502 (18.02.93 93/05)**

(30) Priority: **26.07.91 JP 187602/91**

(43) Date of publication of application: **14.07.93 Bulletin 93/28**

(84) Designated Contracting States: **DE FR GB**

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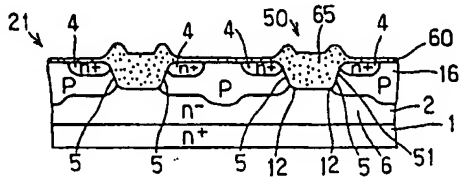
(54) METHOD OF PRODUCING VERTICAL MOSFET.

(57) A vertical power MOSFET which has a markedly decreased on-resistance per unit area. A groove having a gate structure is substantially formed by the LOCOS method prior to forming the p-type base layer and the n^+-type source layer. Then, the p-type base layer (16) and the n^+-type source layer (4) are formed by double diffusion being self-aligned with the LOCOS oxide film (65) and, at the same time, a channel (5) is set in the sidewall (51) of the LOCOS oxide film. Then, the LOCOS oxide film is removed to form a U-groove thereby to constitute the gate structure. That is, the channel is set by double diffusion which is self-aligned to the LOCOS oxide film, i.e., the channels are correctly set symmetrically in the sidewalls on both sides of the groove. Therefore, the position of the U-groove is not deviated with respect to the end of the base layer, and the length of the bottom surface of the U-groove can be minimized. This makes it possible to greatly decrease the size of the unit cell and to greatly decrease the on-resistance per unit area.

FIG.9



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Technical Field

The present invention relates to a vertical type MOSFET (Metal Oxide Semiconductor Field Effect Transistor) to be used as a semiconductor device for electric power, which is preferable in the case of adoption as MOSIC and the like in which an elemental article thereof or the semiconductor device for electric power is incorporated.

Background Art

The vertical type power MOSFET has many features such that it has excellent frequency characteristics, has a fast switching velocity, can be driven at low electric power and the like, so that it is recently used in many industrial fields. For example, in "Nikkei Electronics" published by Nikkei-McGraw-Hill, Inc. on May 19, 1986, pp. 165-188, it is described that the focus of development of the power MOSFET is migrating to low voltage resistant articles and high voltage resistant articles. Further, it is described in this literature that the ON-resistance of a power MOSFET chip having a voltage resistance not more than 100 V has become low up to a level of 10 mΩ, and it is described as a reason thereof that the channel width per area has been able to be made large by utilizing the fine processing of LSI in the production of the power MOSFET, or by improving the shape of its cell. In addition, in this literature, the description is made using the vertical type power MOSFET as a main topic in which a DMOS type (double diffusion type) cell which is in the main current is used. The reason is that the DMOS type is fabricated by the planar process characterized in that the flat main surface of a silicon wafer is exactly used for a channel portion, so that it has advantages in production of a good yield and a cheap cost.

On the other hand, in accordance with popularization of the vertical type power MOSFET, the realization of low loss and low cost is further demanded, however, the reduction in the ON-resistance by the fine processing or the improvement in the shape of the cell has arrived at the limit. For example, according to the official gazette of Japanese Patent Application Laid-open No. Sho 63-266882 (1988), it has been known that the DMOS type has a local minimum point in which the ON-resistance does not further decrease even when the size of the unit cell is made small by the fine processing, and a major cause thereof is the increase in the JFET resistance which constitutes a component of the ON-resistance. In addition, with respect to the DMOS type, as shown in the official gazette of Japanese Patent Application Laid-open No. Hei 2-86136 (1990), the size of the unit cell with which the ON-resistance provides the local minimum point is in the vicinity of 15 μm under the present fine processing technique.

In order to break through this limit, various structures have been proposed. The common feature among them is a structure in which a groove is formed on the device surface, and channel portions are formed at side faces of the groove, and owing to this structure, the above-mentioned JFET resistance can be greatly decreased. Further, in the structure in which the channel portions are formed at the side faces of the groove, the increase in the JFET resistance can be neglected even when the unit cell size is made small, so that there is no limit that the ON-resistance provides the local minimum point with respect to the reduction in the unit cell size as described in the official gazette of Japanese Patent Application Laid-open No. Sho 63-266882 (1988), and it can be made small to the limit of the fine processing breaking though 15 μm.

The structure, in which the channel portions are formed at the side faces of the groove, is called the R (Rectangular)-MOS or the U (U-shaped)-MOS according to its shape. The structure shown in the official gazette of Japanese Patent Application Laid-open No. Sho 59-8743 (1984) is an example of the R-MOS, which is a structure alternatively called the trench gate type in which a vertical groove is formed at the device surface by means of the anisotropic dry etching method, and channels and a gate are formed at sidewall portions of this groove, and this can completely extinguish the JFET resistance component. On the other hand, the structure shown in the official gazette of Japanese Patent Application Laid-open No. Hei 2-86171 (1990) is an example of the U-MOS in which the anisotropic wet etching of silicon or the LOCOS oxidation (Local Oxidation of Silicon) method is used as a method for processing the channel portion into the U-groove shape, and this can also greatly reduce the JFET resistance component.

Typical conventional examples of the vertical type power MOSFET in which the channel portions are formed at the side faces of the groove are shown in Fig. 14 (R-MOS) and Fig. 15 (U-MOS).

At first, the R-MOS shown in Fig. 14 will be explained. In this vertical type power MOSFET, at the surface layer portion of an epitaxial layer 2 comprising an n^--type layer provided on a main face of a semiconductor substrate 1 comprising an n^+-type silicon, a p-type diffusion layer and an n^+-type diffusion layer are successively formed by ion implantation and thermal diffusion. Next, in order to allow parts of these p-type diffusion layer and n^+-type diffusion layer to remain as a p-type base layer 16 and an n^+-type

source layer 4 respectively, the reactive ion etching method is used to perform etching until the penetration though the p-type diffusion layer in the vertical direction with respect to the silicon substrate, so as to form a trench groove 50. A gate oxide film 8 is formed on an inner wall 51 of this trench groove 50, on which a gate electrode 9 is formed. Thus channels 5 are formed at sidewall portions of the inner wall 51, and the channel length is determined by a thickness of the p-type base layer 16. The ohmic contact is made for a source electrode 19 with the n^+-type source layer 4, and for a drain electrode 20 with the back face of the semiconductor substrate 1, respectively.

In this R-MOS, the ON-resistance between the drain and the source thereof is approximately the same as a sum of a channel resistance and a resistance of the n^--type drain layer 6, in which there is no JFET resistance which has been a problem in the above-mentioned DMOS type. Therefore, the ON-resistance monotonously decreases in accordance with the reduction in the unit cell size a'', the reduction can be made up to 5 to 6 μm which is the limit in the present fine processing, and the ON-resistance per area can be greatly reduced as compared with the DMOS type.

However, the R-MOS has such drawbacks that the yield and the reliability are low. The cause is that the trench groove 50 is formed by the reactive ion etching method, so that the flatness of the sidewall surface of the inner wall 51 is bad to give many defects, and the film quality of the gate oxide film 8, which is formed by oxidizing the surface thereof, is bad. And the insulation inferiority of the gate oxide film, the decrease in the mobility due to the defect of the interface of the channel portion, and the change in the threshold voltage take place. As described above, the structure of the R-MOS has the advantage to greatly reduce the ON-resistance per area, whereas there are a problem of high cost resulting from the low yield, and a problem of difficulty to ensure the reliability due to the bad stability of the gate oxide film and the channel portion.

On the contrary, in the U-MOS shown in Fig. 15, the anisotropic wet etching or the LOCOS oxidation method is used as the step for forming the U-groove instead of the reactive ion etching, so that the flatness of the sidewall surface is good, a U-groove 50 having an inner wall 51 with less defect can be formed, and the film quality of a gate oxide film 8 formed by oxidizing the surface thereof is also good. As a result, as for the fact that no insulation inferiority occurs, the characteristics of the channel portion can be made stable and the like, the vertical type power MOSFET having a high yield and reliability can be obtained.

Fablication steps for this U-MOS will be explained in accordance with Fig. 16 to Fig. 19 and Fig. 15. In this vertical type power MOSFET, as shown in Fig. 16, using a mask of an insulation film 22 partially formed with a cycle of a size a' of a cell on the main surface of a wafer 21 provided with an epitaxial layer 2 comprising an n^--type layer provided on a main face of a semiconductor substrate 1 comprising n^+-type silicon, boron is doubly diffused by selective ion implantation and thermal diffusion, so as to form a p-type diffusion layer 23 and a p^+-type contact region 17. Next, after removing the insulation film 22, as shown in Fig. 17, using a mask of an insulation film 24 partially formed on the main surface of the wafer 21, phosphorus is diffused so as to form an n^+-type diffusion layer 25 to overlap over p-type diffusion layers 23 of adjacent cells 15.

Next, after removing the insulation film 24, as shown in Fig. 18, using a mask of an insulation film 26 partially formed on the main surface of the wafer 21, the U-groove 50 is formed by the anisotropic etching or the LOCOS oxidation method. By the formation of this U-groove 50, peripheral edge portions of the adjacent p-type diffusion layers 23 and the central portion of the n^+-type diffusion layer 25 are removed, so as to form a p-type base layer 16 and an n^+-type source layer 4 separated by the U-groove 50 for every unit cell having a unit cell size of a'.

Next, after removing the insulation film 26, as shown in Fig. 19, a gate oxide film 8 is formed on the surface of the U-groove 50, and a gate electrode 9 comprising polysilicon is formed on this gate oxide film 8. Next, as shown in Fig. 15, an interlayer insulation film 18 is formed on the main surface of the wafer 21 so as to cover the gate oxide film 8 and the gate electrode 9, and the interlayer insulation film 18 is subjected to opening formation in order to expose parts of the p^+-type base contact layer 17 and the n^+-type source layer 4. A source electrode 19, which makes ohmic contact with the p^+-type base contact layer 17 and the n^+-type source layer 4, is formed on the main surface of the wafer 21. Further, a drain electrode 20 which makes ohmic contact with the back face of the semiconductor substrate 1 is formed, and the vertical type power MOSFET of the U-MOS structure is completed.

This U-MOS shown in Fig. 15 has the feature that the yield and the reliability are high in a degree equivalent to the DMOS type, which is extremely excellent in this point as compared with the R-MOS. This is due to the fact that the U-groove 50 is formed by the wet etching of silicon or the LOCOS oxidation method, thereby the flatness of its inner wall 51 is good with less defect, and the film quality of the gate oxide film 8 formed by oxidizing the surface thereof is also good, and it becomes difficult to cause the insulation inferiority of the gate oxide film and the characteristic change of the channel portion.

The ON-resistance between the drain and the source of the U-MOS is approximately the same as a sum of a channel resistance and a resistance of the n^--type drain layer 6 in the same manner as the above-mentioned R-MOS, and the JFET resistance of a JFET portion 7 is sufficiently small. Thus, in the same manner as the above-mentioned R-MOS, the ON-resistance decreases monotonously in accordance with the reduction in the unit cell size a', however, it can be only made slightly smaller than about 15 μm of the DMOS type within the limit of the present fine processing, and cannot be made small into 5 to 6 μm of the R-MOS type. However, since the JFET resistance is sufficiently small, the ON-resistance per area is an intermediate value between those of the R-MOS type and the DMOS type. As described above, the U-MOS has such a structure in which the feature of the low ON-resistance of the R-MOS is partially inherited while maintaining the high production yield and the high reliability of the DMOS.

In order to reduce the ON-resistance of the U-MOS to be equivalent to the R-MOS, it is necessary and indispensable to reduce the unit cell size a'. However, in the production method of the U-MOS shown in Figs. 16 to 19 and Fig. 15, the reduction in the unit cell size a' is difficult. The reason thereof will be explained hereinafter.

At first, it will be explained in detail that by what the unit cell size of the U-MOS is determined.

In Fig. 15, sizes of each of portions have relations as shown as follows.

$$\begin{aligned} a' &= b' + 2\alpha' \\ b' &= c' + 2\beta' \\ c' &= d' + 2\gamma' \\ d' &= e' + 2\delta' \end{aligned} \qquad \cdots(1)$$

However, a' is a unit cell size, b' is a distance between upper ends of two adjacent U-grooves, c' is a distance between adjacent gate electrodes, d' is a size of a contact hole, and e' is a size of a portion of the base contact layer 17 exposed to the surface. In addition, α' is a plane distance between the center and the upper end of the U-groove 50, β' is a plane distance between the upper end of the U-groove 50 and the end of the gate electrode 9, γ, is a plane distance between the end of the gate electrode 9 and the end of the contact hole, and δ' is a plane distance between the end of the contact hole and the end of the portion of the base contact layer 17 exposed to the surface.

In this case, in the present fine processing level, the adjustment accuracy of the mask is about 0.5 to 1 μm, and also considering the size accuracy in the etching processing and the like, each value in the above-mentioned formulae (1) takes, for example, the following value.

$\beta' = 1$ [μm], $\gamma' = 1.5$ [μm], $\delta' = 1$ [μm], $b' = 8.5$ [μm], $c' = 6.5$ [μm], $d' = 3.5$ [μm], $e' = 1.5$ [μm] - (2)

According to the formulae (1) and (2), the unit cell size a' is

$$a' = b' + 2\alpha' = 8.5 + 2\alpha' \text{ [μm]} \quad (3)$$

wherein in order to reduce the unit cell size a', the value of the plane distance α' between the center and the upper end of the U-groove 50 is key.

According to Figs. 16 to 18, it is understood that the size of α' is determined by the length of the bottom side and the processing accuracy of the U-groove 50, and the adjustment accuracy of the insulation film 26 (the mask for forming the U-groove) with respect to the p-type diffusion layer 23. Fig. 20 is a cross-sectional view of an important part including the U-groove 50 when a center line CL_1 between the two adjacent p-type diffusion layers 23 overlaps a center line CL_2 between the two adjacent insulation films 26, which corresponds to a case in which there is no mask deviation. In this case, α' is given by the following formula (4).

$$\alpha' = \alpha'_1 + \alpha'_2 + \alpha'_3 \quad (4)$$

However, α'_1 is 1/2 of a length with which the bottom side portion of the U-groove 50 contacts with the n^--type drain layer 6, α'_2 is a length with which the bottom side portion of the U-groove 50 contacts with

the p-type base layer 16, and α'_3 is a length of projection of the sidewall portion of the U-groove 50 onto the main surface of the wafer 21.

In this case, the right and left α'_2s are apparently equal in Fig. 20. However, in fact, due to the presence of the deviation of the mask adjustment, the right and left α'_2s are different, so that it is necessary that α'_2 in each of the items in the formula (4) is set to be about 1.5 μm. The reason thereof is that when the mask adjustment of the insulation film 26 is the worst, on account of the mask adjustment accuracy in the present circumstance, as shown in Fig. 21, with respect the center line CL_1 between the two adjacent p-type diffusion layers 23, the center line CL_2 between the two adjacent insulation films 26 generates positional deviation (for example, 1 μm) in the right direction, and in order to prevent electric field concentration at the edge portion 12 so as to avoid the inconvenience resulting from dielectric breakdown of the gate portion even when such positional deviation takes place, for allowing the edge portion 12 at the groove bottom of the U-groove 50 not to be exposed to the n^--type drain layer 6 but to be positioned in the p-type base layer 16, it is necessary to make a design in which this positional deviation is taken into account. Therefore, the following formula (5) must be necessarily established with respect to lengths α'_{21} and α'_{22} with which the bottom side portions of the U-groove 50 contact with the p-type base layers 16.

$$0 < \alpha'_{21}, \alpha'_{22} \quad (5)$$

In addition, with respect to α'_1 and α'_3, both of them are about 0.75 μm in the present fine processing level, so that α' takes the following value according to the formula (4).

$$\alpha' = 0.75 + 1.5 + 0.75 = 3\ [\mu m] \quad (6)$$

Therefore, according to the formulae (3) and (6), the minimum value of the unit cell size a' is

$$a' = 8.5 + 2 \times 3 = 14.5\ [\mu m] \quad (7)$$

As described above, in the production method of the U-MOS shown in Figs. 16 to 19 and Fig. 15, the reduction limit of the unit cell size a' is about 14.5 μm, which is approximately the same as 15 μm of the conventional DMOS type, and it has been difficult to remarkably reduce the ON-resistance per area.

It is an object of the present invention to provide a vertical type power MOSFET in which the ON-resistance can be made small.

Disclosure of Invention

In order to achieve the above-mentioned object, the production method of a vertical type power MOSFET according to the present invention is different from conventional methods, which lies in such a basic concept that substantial groove formation is performed beforehand before formation of a base layer and a source layer.

Namely, the summary thereof may be briefly explained such that the production method of a vertical type MOSFET according to the present invention is characterized in that it comprises

a local oxidation step which includes a step of preparing a semiconductor substrate, a step of formimg a semiconductor layer of the first conductive type at one main face side of the semiconductor substrate, the semiconductor layer having an impurity concentration lower than that of the semiconductor substrate and using the surface of the semiconductor layer of the low concentration as a main surface, and a step of local oxidizing a predetermined region of the main surface, thereby a local oxide film having a predetermined depth from said main surface is formed in said semiconductor layer in the predetermined region,

an impurity introduction step in which in order to form channels on said semiconductor layer surface contacting with a side face of said local oxide film, impurities of the second conductive type and the first conductive type are doubly diffused from said main surface successively in a manner of self-alignment with respect to said local oxide film, and the length of said channel is determined by the double diffusion, simultaneously with which a base layer of the second conductive type and a source layer of the first conductive type are formed, and remained said semiconductor layer is made into a drain layer of the first conductive type,

a gate formation step in which said local oxide film is removed after the double diffusion to form a groove structure having said predetermined depth, an inner wall of said groove including a portion to become said channel is oxidized to provide a gate oxide film, and a gate electrode is formed on the gate oxide film, and

a source and drain electrodes formation step in which a source electrode which electrically contacts with both said source layer and said base layer, and a drain electrode which electrically contacts with the other main face side of said semiconductor substrate are formed.

Namely, the base layer and the source layer are formed by the double diffusion in a manner of self-alignment using the local oxide film as the mask for diffusion, simultaneously with which the channel region is set at the sidewall portion of the semiconductor layer subjected to erosion by the local oxide film. In addition, this local oxide film is removed in the following steps, which becomes the groove portion in which the gate electrode is established.

As described above, the channels are formed at the sidewall portions in the manner of self-alignment by the end face of the local oxide film, so that the channels of the adjacent cells formed at each of the sidewall portions of the grooves have an exactly symmetric structure. In addition, the base layer is diffused in the manner of self-alignment using the local oxide film as the mask, so that the base layer is subjected to the diffusion and formation with exact positional determination at the sidewall portion of the groove, and its conjugation depth can be exactly controlled. Therefore, it is also possible to set a diffusion condition so as to allow the base layer to exactly wrap the edge portion of the groove bottom face.

As described above, the groove is formed by the local oxidation method, and the local oxide film is used as the mask to form the base layer, the source layer and the channel by the double diffusion in the manner of self-alignment, thereby the edge portion of the groove bottom side can be made into an exactly symmetric structure in each cell.

Therefore, it is unnecessary to form a U-groove having a sufficiently long bottom face to allow the edge portion to be positioned in the base layer even when the positional deviation of the U-groove with respect to the base layer end occurs as in the conventional U-MOS, and the length of the bottom face of the U-groove can be made short into the necessary minimum. As a result, it is unnecessary to take the mask deviation into account, the unit cell size can be greatly reduced, and the ON-resistance per area can be reduced to be approximately the same as that of the R-MOS. Moreover, the production yield and the reliability are high in a degree equivalent to the DMOS type.

Brief Description of Drawings

Fig. 1 (a) is a plane view showing a part of a vertical type power MOSFET according to the first example of the present invention, Fig. 1 (b) is a cross-sectional view taken along A-A in Fig. 1 (a), and Fig. 2 to Fig. 13 are cross-sectional views of important parts to be used for the explanation of production steps of the vertical type power MOSFET according to the first example of the present invention.

Fig. 14 is a cross-sectional view of a vertical type power MOSFET of the conventional R-MOS type, Fig. 15 is a cross-sectional view of a vertical type power MOSFET of the conventional U-MOS type, and Fig. 16 to Fig. 19 are cross-sectional views of important parts to be used for the explanation of production steps of the vertical type power MOSFET of the conventional U-MOS type. Fig. 20 is a cross-sectional view of an important part showing an ideal state in which the positional relation between an edge portion of a groove bottom face and a p-type base layer is in bilateral symmetry when the groove is formed in the production of the vertical type power MOSFET of the conventional U-MOS type. Fig. 21 is a cross-sectional view of an important part showing a practical state in which the positional relation between the edge portion of the groove bottom face and the p-type base layer is not in bilateral symmetry due to mask deviation when the groove is formed in the production of the vertical type power MOSFET of the conventional U-MOS type.

Fig. 22 is a cross-sectional view of an important part of a vertical type power MOSFET according to the second example of the present invention, Fig. 23 (a) is an illustrative plane view showing a part of a vertical type power MOSFET according to the fourth example of the present invention, and Fig. 23 (b) is a cross-sectional view taken along B-B in Fig. 23 (a).

Best Mode for Carrying out the Invention

Examples of the present invention will be explained hereinafter with reference to the drawings.

Fig. 1 (a) is a plane view of a vertical power MOSFET comprising rectangular unit cells according to the first example of the present invention, and (b) in the same figure is a cross-sectional view taken along A-A in the same figure (a). Fig. 2 to Fig. 13 are also cross-sectional views of a wafer as a work in each step in the production of the vertical type power MOSFET, which correspond to Fig. 1 (b). Incidentally, Fig. 2 is a cross-sectional view of the wafer subjected to boron ion implantation for the formation of the central portion of a p-type base layer, Fig. 3 is a cross-sectional view of the wafer subjected to patterning of a silicon nitride film at an interval of a unit cell size a for the LOGOS oxidation, Fig. 4 is a cross-sectional view of the

wafer in which a window of the silicon nitride film is subjected to wet etching, Fig. 5 is a cross-sectional view of the wafer in which a LOGOS oxide film is formed, Fig. 6 is a cross-sectional view of the wafer subjected to boron ion implantation for the formation of the p-type base layer using the LOGOS oxide film as a mask, Fig. 7 is a cross-sectional view of the wafer in which the p-type base layer is formed by thermal diffusion, Fig. 8 is a cross-sectional view of the wafer subjected to phosphorus ion implantation for the formation of an n^+-type source layer using the LOGOS oxide film as a mask, Fig. 9 is a cross-sectional view of the wafer in which the n^+-type source layer is formed by thermal diffusion, Fig. 10 is a cross-sectional view of the wafer in which a gate oxide film is formed by thermal oxidation after removing the LOGOS oxide film, Fig. 11 is a cross-sectional view of the wafer in which a gate electrode is formed on the gate oxide film, Fig. 12 is a cross-sectional view of the wafer subjected to boron ion implantation for the formation of a p^+-type base contact layer, Fig. 13 is a cross-sectional view of the wafer in which the p^+-type base contact layer is formed by thermal diffusion, and Fig. 1 (b) is a completed cross-sectional view of the wafer in which an interlayer insulation film, a source electrode and a drain electrode are formed.

The vertical type power MOSFET of this example has its important part, that is the unit cell portion which has a structure as shown in Fig. 1, which has a structure in which a large number of the unit cells 15 are regularly arranged vertically and laterally on a plane with a pitch width (unit cell size) a.

In Fig. 1, a wafer 21 comprises a semiconductor substrate 1 and an n^--type epitaxial layer 2 thereon. The semiconductor substrate 1 is constituted of n^+-type silicon having an impurity concentration of about 10^{20} cm^{-3} and a thickness of 100 to 300 μm and the n^--type epitaxial layer 2 has an impurity concentration of about 10^{15} cm^{-3} and a thickness of about 7 μm. And the unit cells 15 are constituted on the main surface of this wafer 21. In order to form a U-groove 50 on the main surface of the wafer 21 with a unit cell size a of about 12 μm, a LOGOS oxide film having a thickness of about 3 μm is formed, and using this oxide film as a mask, the double diffusion in a manner of self-alignment is used to form a p-type base layer 16 having a junction depth of about 3 μm and an n^+-type source layer 4 having a junction depth of about 1 μm, thereby a channel 5 is set at a sidewall portion 51 of the U-groove 50. Incidentally, the junction depth of the p-type base layer 16 is set to be a depth with which no destruction occurs due to breakdown at an edge portion 12 of the bottom side of the U-groove 50. In addition, in order to allow the junction depth of the central portion of the p-type base layer 16 to be deeper than those of surroundings, boron is beforehand diffused at the central portion of the p-type base layer 16, so as to be set to allow the breakdown to occur at the central portion of the bottom face of the p-type base layer 16 when a high voltage is applied between the drain and the source. In addition, after the double diffusion, the diffusion mask and the LOGOS oxide film used for the formation of the U-groove 50 are removed, a gate oxide film 8 having a thickness of about 60 nm is formed at the inner wall of the U-groove 50, and a gate electrode 9 comprising polysilicon having a thickness of about 400 nm and an interlayer insulation film 18 comprising BPSG having a thickness of about 1 μm are formed thereon. Further, at the surface of the central portion of the p-type base layer 16, a p^+-type base contact layer 17 having a junction depth of about 0.5 μm is formed, and a source electrode 19 formed on the interlayer insulation film 18 makes ohmic contact with the n^+-type source layer 4 and the p^+-type base contact layer 17 through the contact hole. In addition, a drain electrode 20 is formed to make ohmic contact with the back face of the semiconductor substrate 1.

In the vertical type power MOSFET of the present example shown in Fig. 1 as explained above, the LOGOS oxide film is used as the mask to doubly diffuse the p-type base layer 16 and the n^+-source layer 4 by the self-alignment, so that it becomes unnecessary to take the adjustment accuracy of the mask into account, and in the above-mentioned formulae (1) to (7) established in the conventional U-MOS shown in Fig. 15, the length α_2' to contact with the p-type base layer 16 of the bottom side portion of the U-groove 50 can be neglected. Therefore, when each of the sizes other than α_2' is the numerical value as the prior art shown in the numerical formula 2, then in the present example, according to the formula (7), the plane distance α between the center and the upper end of the U-groove 50 can be reduced from 3 μm up to 1.5 μm.

As a result, the unit cell size a can be reduced up to 11.5 μm from 14.5 μm of the conventional U-MOS shown in Fig. 15, and the channel width per area can be taken widely, to make it possible to reduce on-resistance up to a value near the ON-resistance per area of the R-MOS shown in Fig. 14.

Next, a production method of the vertical type power MOSFET according to the present invention will be explained.

At first, as shown in Fig. 2, a wafer 21, in which an n^--type epitaxial layer 2 is grown on the main surface of a semiconductor substrate 1 comprising n^+-type silicon, is prepared. This semiconductor substrate 1 has its impurity concentration of about 10^{20} cm^{-3}. In addition, the epitaxial layer 2 has its thickness of about 7 μm and its impurity concentration of about 10^{15} cm^{-3}. The main surface of this wafer 21 is thermally oxidized to form a field oxide film 60 having a thickness of about 60 nm, and then a

photoresist film 61 is deposited to perform patterning of the photoresist film 61 into a pattern opening to the central portion of a planned position of cell formation by means of known optical lithography steps. And using this photoresist film 61 as a mask, ion implantation of boron (B^+) is performed.

After peeling off the resist, a p-type diffusion layer 62 having a junction depth of about 3 μm is formed by thermal diffusion as shown in Fig. 3. This p-type diffusion layer 62 ultimately becomes a part of a p-type base layer 16 as described hereinafter, and when a high voltage is applied between the drain and the source, the breakdown is allowed to occur stably at the bottom side portion of the p-type diffusion layer 62, thereby an object to increase the surge resistance is achieved.

Next, as shown in Fig. 3, a silicon nitride film 63 is deposited on the main surface of the wafer 21 by about 200 nm, and this silicon nitride film 63 is subjected to patterning to form an opening pattern of a lattice shape opening with a pitch width (size of the unit cell 15) a. Incidentally, this opening pattern is subjected to mask adjustment so as to allow the above-mentioned p-type diffusion layer 62 to be positioned at the central portion of its pitch interval.

Next, as shown in Fig. 4, the silicon nitride film 63 is used as a mask to etch the field oxide film 60, subsequently the n^--type epitaxial layer 2 is etched into a depth of about 1.5 μm to form a groove 64.

Next, as shown in Fig. 5, the silicon nitride film 63 is used as a mask to thermally oxidize the portion of the groove 64. This is an oxidation method well-known as the LOGOS (Local Oxidation of Silicon), and a LOGOS oxide film 65 is formed by this oxidation, simultaneously with which a U-groove 50 is formed on the surface of the n^--type epitaxial layer 2 subjected to erosion by the LOGOS oxide film 65, and the shape of the groove 50 is decided. Namely, the distance b between upper ends of the adjacent U-grooves 50 is determined by a size of the silicon nitride film 63, which becomes slightly short due to side face oxidation by the so-called bird's beak. However, this reduction in the size is about 0.5 μm, and it can be controlled with a high accuracy. Incidentally, it is desirable that an inclination angle of the side face of the U-groove 50 with respect to the main surface of the wafer 21 is not less than 45°, which can be controlled by condition setting of the LOGOS oxidation or depth setting of the groove 64 formed prior to the LOGOS oxidation step.

As described hereinafter, the distance b between the upper ends of the adjacent U-grooves 50 is about 8.5 μm. In addition, in Fig. 5, the plane distance α between the center and the upper end of the U-groove 50 is given by the formula (8) in the same manner as the case of the conventional U-MOS to be given by Fig. 20 and the formula (4).

$$\alpha = \alpha_1 + \alpha_2 + \alpha_3 \quad (8)$$

However, α_1 is 1/2 of a length to contact with the n^--type drain layer 6 of the bottom side portion of the U-groove 50, α_2 is a length to contact with the p-type base layer 16 of the bottom side portion of the U-groove 50, and α_3 is a length of projection of the sidewall portion of the U-groove 50 onto the main surface of the wafer 21.

However, α_2 in the formula (8) can be omitted as described hereinafter, so that the formula (8) can be rewritten into the following formula.

$$\alpha = \alpha_1 + \alpha_3 \quad (9)$$

Both α_1 and α_3 are about 0.75 μm in the processing technique in the present circumstance, so that a takes the following value.

$$\alpha = 1.5\ [\mu m] \quad (10)$$

Incidentally, the inner wall surface of the U-groove 50 formed by the LOGOS oxidation is flat and has less defect, and the surface has a good surface state in a degree equivalent to the initial main surface of the wafer 21 shown in Fig. 2.

Next, as shown in Fig. 6, the LOGOS oxide film 65 is used as a mask to perform ion implantation of boron through the thin field oxide film 60 for forming the p-type base layer 16. At this time, the boundary portion between the LOGOS oxide film 65 and the field oxide film 60 makes a self-aligned position, and the region to be subjected to the ion implantation is exactly defined.

Next, as shown in Fig. 7, thermal diffusion is performed to give a junction depth of about 3 μm. Owing to this thermal diffusion, the p-type diffusion layer 62 formed beforehand in the step shown in Fig. 3 is integrated with a diffusion layer of boron implanted in the step shown in Fig. 6, and one p-type base layer 16 is formed. In addition, both end faces of the region of the p-type base layer 16 are defined at the positions of the sidewalls of the U-groove 50 in a manner of self-alignment.

Next, as shown in Fig. 8, using masks of both of the LOGOS oxide film 65 and the photoresist film 66 subjected to patterning with a pattern remained at the surface central portion of the p-type base layer 16 surrounded by the LOGOS oxide film 65 having been formed on the surface of the wafer 21 in the lattice-shaped pattern, ion implantation of phosphorus through the thin field oxide film 60 is performed for forming the n^+-type source layer 4. Also in this case, in the same manner as the case in which boron has been ion-implanted in the step shown in Fig. 6, the boundary portion between the LOGOS oxide film 65 and the field oxide film 60 makes a self-alignment position, and the region to be subjected to the ion implantation is exactly defined.

Next, as shown in Fig. 9, thermal diffusion is performed with a junction depth of 0.5 to 1 μm, so as to form the n^+-type source layer 4 and simultaneously set the channel 5. In this thermal diffusion, the end face of the region of the n^+-type source layer 4 to contact with the U-groove 50 is defined at the position of the sidewall of the U-groove 50 in a manner of self-alignment.

Setting of a junction depth of the p-type base layer 16 at the time point of completion of this thermal diffusion becomes important. Namely, when a high voltage is applied between the drain and the source of a completed article of the vertical type power MOSFET of the present example, it is important to set the junction depth of the p-type base layer 16 at the value not to be destroyed by the occurrence of breakdown at the edge portion 12 of the bottom face of the U-groove 50. This junction depth can be exactly defined by the thermal diffusion.

As described above, in accordance with the steps in Fig. 6 to Fig. 9, the junction depth of the p-type base layer 16 and its shape are decided. The important fact with respect to the shape of this p-type base layer 16 is that the position of the side face of the p-type base layer 16 is self-aligned with the side face of the U-groove 50 and after that thermally diffused so that the shape of the p-type base layer 16 becomes completely bilateral symmetry with respect to the U-groove 50. As a result, the difference between the right and left contact lengths α'_{21} and α'_{22} resulting from the mask deviation of the bottom side portion of the U-groove 50 and the p-type base layer 16, which has occurred in the conventional U-MOS as shown in Fig. 21, always disappears in accordance with the production steps of the present invention, and the following formula is established.

$$\alpha'_{21} = \alpha'_{22} \quad (11)$$

Further, the junction depth of the p-type base layer 16 can be exactly determined by condition setting of the thermal diffusion, so that it becomes unnecessary to take the length α'_2 with which the bottom side portion of the U-groove 50 contacts with the p-type base layer 16 into account. Namely, in the present example, α_2 can be omitted in the above-mentioned formula (8), and hence the above-mentioned formula (9) is established.

Next, as shown in Fig. 10, the LOGOS oxide film 65 is removed by wet etching to make exposure of the inner wall 51 of the U-groove 50, and then the gate oxide film 8 having a thickness of about 60 nm is formed by thermal oxidation. As described above, the inner wall 51 of the U-groove 50 is a good silicon surface having good flatness and less defect, so that the film quality of the gate oxide film 8 made by thermally oxidizing this surface, the interface state density of the interface of the channel 5, and the carrier mobility are good in a degree equivalent to the conventional DMOS.

Next, as shown in Fig. 11, a polysilicon film having a thickness of about 400 nm is deposited onto the main surface of the wafer 21, to form a gate electrode 9 in which patterning is made so as to be separated by the distance c being shorter than the distance b between the upper ends of the two adjacent U-grooves 50 by 2β. Taking the adjustment accuracy of the mask of 0.5 to 1 μm into account, when β is set to be about 1 μm so as to allow the gate electrode 9 to necessarily terminate at the flat portion of the main surface of the wafer 21, the separation distance c between the two adjacent gate electrodes 9 is 6.5 μm.

As described above, the steps shown in Fig. 6 to Fig. 11 are most important parts of the production steps in the present example, wherein the LOGOS oxide film 65 is used as the mask for the double diffusion of the manner of self-alignment, the p-type base layer 16, the n^+-source layer 4 and the channel 5 are formed, and then the LOGOS oxide film 65 is removed, after which the gate oxide film 8 and the gate electrode 9 are formed.

Next, as shown in Fig. 12, using the photoresist film 68 subjected to patterning as a mask, boron is ion-implanted through the oxide film 67 for forming a p^+-type base contact layer 17 .

Next, as shown in Fig. 13, thermal diffusion is performed with a junction depth of about 0.5 μm, and the p^+-type base contact layer 17 is formed. In this thermal diffusion, the size e of exposure of the p^+-type base contact layer 17 to the surface is about 1.5 μm, which is determined by a pattern size of the photoresist film 68.

And as shown in Fig. 1 (b), an interlayer insulation film 18 comprising BPSG is formed on the main surface of the wafer 21, a part of which is subjected to contact hole opening so as to expose the p^+-type base contact layer 17 and the n^+-type source layer 4. Further, a source electrode 19 comprising an aluminum film is formed, so as to make ohmic contact of the p^+-type base contact layer 17 and the n^+-source layer 4 through the above-mentioned contact hole. Further, for protection of the aluminum film, a passivation film (not shown in the figure) comprising silicon nitride or the like is formed by the plasma CVD method or the like, and a drain electrode 20 comprising three-layer film of Ti/Ni/Au is formed on the back face of the wafer 21, so as to make ohmic contact with the n^+-type semiconductor substrate 1.

As described above, in the structure and the production method of the vertical type power MOSFET according to the present example explained using Fig. 2 to Fig. 13 and Fig. 1, the following effects are provided.

(1) As compared with the conventional U-MOS shown in Fig. 15, a different factor among the conditions for determining the unit cell size a given by the formula (1) to the formula (7) is α shown by the formula (9) and the formula (10), which can be reduced into 1.5 μm from conventional 3 μm. As a result, according to the formula (3), the unit cell size a can be reduced from conventional 14.5 μm up to a value given by the following formula (12), and it is possible to allow the ON-resistance per area to further approach that of the R-MOS.

$$a = 8.5 + 2 \times 1.5 = 11.5\ [\mu m] \quad (12)$$

(2) The silicon surface on which the channel portion is formed is the silicon surface made by removing the oxide film formed by the LOGOS oxidation method by means of the wet etching, wherein the flatness of the surface is good, and there is no defect at all. Therefore, in relation to the film quality of the gate oxide film made by thermally oxidizing this surface, the problems of the insulation inferiority, the decrease in the mobility due to defect of the interface of the channel portion, the change in the threshold voltage and the like are small in a degree equivalent to the conventional DMOS type. As a result, the yield is high and the reliability is high.

(3) Methods in which delicate management is required in production steps as represented by the reactive ion etching in the R-MOS are not used, but the LOGOS oxidation method, in which management of production is extremely easy and the size accuracy and the reproducibility are good, is used, so that the throughput and the yield in the production steps are high, and the production cost is also cheap.

As described above, the present invention has been concretely explained on the basis of the above-mentioned first example, however, it is needless to say that the present invention is not limited to the above-mentioned example, which can be variously changed within a range without deviating from the gist thereof.

For example, in the second example shown in Fig. 22, a source electrode 19 is allowed to make ohmic contact with an n^+-type source layer 4 and a p^+-type base contact layer 17 through a groove 52, and especially there is given a structure in which the source electrode 19 makes ohmic contact with the side face of the n^+-type source layer 4. In order to fabricate this structure, in the production steps shown in Fig. 2 to Fig. 13, the n^+-source layer 4 is diffused and formed on the whole face of the upper face of the p-type base layer 16 to constitute the gate structure, and further when the contact hole is opened through the interlayer insulation film 18, a groove 52 may be formed penetrating through the interlayer insulation film 18 and the n^+-type source layer 4 to arrive at the p^+-type base contact layer 17. Incidentally, setting can be made variously such that the p^+-type base contact layer 17 is formed beforehand before the formation of the n^+-type source layer 4, is formed by performing ion implantation of boron with increasing the acceleration voltage after the formation of the n^+-type source layer 4, is formed simultaneously with the n^+-type source layer 4 by thermal diffusion using ion implantation of boron before thermal diffusion for the formation of the n^+-type source layer or the like.

According to this structure, it becomes unnecessary to take the plane distance δ between the end of the contact hole and the end of the portion of exposure of the base contact layer 17 to the surface into account in Fig. 1 (b). Further, it is unnecessary to especially define the size e of the portion of exposure of the base contact layer 17 to the surface, and when the contact hole having a size of d is opened, the base contact layer 17 can be simultaneously exposed. Namely, according to the structure and the production method of the present second example, a part of the formula (1) to the formula (3) in relation to the conventional U-MOS is changed as follows.

$$d''' = 1.5\ [\mu m]$$
$$c''' = 4.5\ [\mu m]$$
$$b''' = 6.5\ [\mu m] \qquad \ldots(13)$$
$$a''' = b''' + 2\alpha$$

Therefore, according to the formula (13) and the formula (10), the unit cell size of the vertical type power MOSFET can be made small into not more than 10 μm as

$$a''' = 6.5 + 2 \times 1.5 = 9.5\ [\mu m] \qquad (14)$$

the cell size equivalent to the conventional R-MOS becomes possible, and remarkable reduction in the ON-resistance can be contemplated. Moreover, in the same manner as the first example, the vertical type power MOSFET in which the yield and the reliability are high is obtained.

Next, the third example of the present invention will be explained. In the following explanation, referring to the production method of the vertical type power MOSFET according to the first example of the present invention and its structural figures shown in Fig. 1 to Fig. 13, the explanation is made being limited to portions in which the present third example is different from the above-mentioned first example or portions which are newly set in the third example, and since the other portions are the same as those of the above-mentioned first example, their explanation will be omitted.

In the third example, in Fig. 2, the wafer 21 is selected to have the index of plane of its main surface which is (1 1 1) or those near it. Thus the surface of the n^--type epitaxial layer 2 corresponding to the bottom face of the LOGOS oxide film 65 formed on the wafer 21 in the step shown in Fig. 5, that is the bottom face 53 of the U-groove 50 is parallel to the main surface, so that its index of plane is also (1 1 1).

In addition, in Fig. 1 (a), owing to the optimization of the surface directions of the sides of the rectangular unit cell 15 with respect to the surface direction of the main surface of the wafer 21, and the optimization of the inclination angle of the side face 54 of the U-groove 50 by condition setting in the LOGOS oxidation step shown in Fig. 5, the index of plane of the side face 54 of the U-groove 50 is set to be an index near (1 0 0) in which the interface state density is less.

Thus in the step for forming the gate oxide film 8 shown in Fig. 10, depending on the difference in the index of plane between the bottom face 53 (the index of plane is (1 1 1) as described above) of the U-groove 50 and the side face 54 (the index of plane is an index near (1 0 0) as described above), a step condition is selected in which the oxidation velocity is faster at the bottom face 53. Namely, a relatively rapid oxidation time in which the oxidation of silicon is controlled by rate-determination of reaction and a thin oxide film are necessary conditions, wherein the thin gate oxide film formation of about 60 nm satisfies the conditions. According to the conditions, the thickness t_B of the gate oxide film formed on the surface of the bottom face 53 of the U-groove 50 becomes thicker than the thickness t_S of the gate oxide film formed on the surface of the side face 54 of the U-groove 50. Namely, there is given

$$t_S < t_B \qquad (15)$$

for example, following numerical values are obtained as t_S and t_B.

$$t_S = 60\ [nm],\ t_B = 80\ [nm] \qquad (16)$$

Next, the function will be explained in which the third example is superior to the first example owing to its modification of its structure.

In the third example, as shown in the formulae (15) and (16), the thickness t_B of the gate oxide film formed on the surface of the bottom face 53 of the U-groove 50 in Fig. 1 can be made thicker than the thickness t_S of the gate oxide film formed on the surface of the side face 54 of the U-groove 50. Thus, even when a high voltage is applied between the drain electrode 20 and the source electrode 19, the electric field in the gate oxide film formed at the surface of the bottom face 53 of the U-groove 50 can be reduced, and the dielectric breakdown of the gate oxide film can be prevented. In addition, the gate input capacity of the bottom face portion of the U-groove 50 constituted by the bottom face 53 of the U-groove 50, the gate oxide film formed on its surface and the gate electrode 9 decreases in inverse proportion to the thickness of

the gate oxide film, so that high-speed switching becomes possible.

In addition, in the third example, the index of plane of the side face 54 of the U-groove 50 is set to be an index near (1 0 0) in which the interface state density is less so as to provide a low interface state density of the channel portion 5, so that the stability of the threshold voltage is good, the mobility of the channel portion is not decreased, and the resistance to the hot carrier is also strong, so that the long-term reliability in electric characteristics of the vertical type power MOSFET can be maintained.

As described above, in the third example, since the explanation has been made only for the case of the rectangular unit cell shown in Fig. 1 (a), it was impossible to set index of planes of all of the side faces 54 of the U-groove 50 to be the (1 0 0) plane. The cause thereof is due to the fact that plane (1 1 1) lies in three-times axial symmetry because of its crystal structure, which did not match the rectangular unit cell with no three-times axial symmetry. The fourth example in which this has been improved is shown in Fig. 23. Incidentally, Fig. 23 (a) is an illustrative plane view showing a part of a vertical type power MOSFET according to the fourth example of the present invention, wherein the surface pattern of a gate electrode 9 is given by indication of a part only (the hatched area in the figure) in order to see the figure more easily, and indication of a source electrode 19 is omitted. In addition, Fig. 23 (b) is a cross-sectional view taken along B-B in Fig. 23 (a). In the figure, the same constitution as that in Fig. 1 is designated by the same symbol.

In the fourth example, as shown in Fig. 23 (a), a pattern of a triangular unit cell 15 and a U-groove 50 of a triangular pattern are used, and a face direction of one side of the triangle is set to be ⟨2 1 1⟩, and further as shown in Fig. 23 (b), in order to provide an angle of 54.7° formed by the main surface of a wafer 21 and a side face 54 of the U-groove 50, the conditions in the LOGOS oxidation step shown in Fig. 5 are set. By doing so, index of planes of all of the side faces 54 of the U-groove 50 can be made (1 0 0) in which the interface state is the smallest, and it is possible to form channels having good characteristics equivalent to those of DMOSFET of the conventional planar type.

As described above, in the various examples explained, the explanation has been made only for the case in which the present invention is applied to the vertical type power MOSFET which performs the unipolar operation, however, there is no limitation thereto, and the application may be available to a power MOSIC in which such a vertical type power MOSFET is incorporated, and further the application is also possible to a gate structure of an insulation gate type bipolar transistor (IGBT) which performs the bipolar operation.

In addition, the explanation has been made only for the n-channel type in the examples, however, it is needless to say that the same effect can be obtained with respect to the p-channel type in which the type of the semiconductor is exchanged between the n-type and the p-type.

Further, the plane shape of the unit cell is not limited to the above-mentioned square and the equilateral triangle, and alternatively it is possible to optionally select rectangles, hexagons and the like. Incidentally, with respect to the change of the plane pattern, the change can be easily made using the formation pattern of the LOGOS oxide film 65.

Industrial Applicability

As described above, in the vertical type MOSFET according to the present invention, it is unnecessary to form a U-groove having a sufficiently long bottom face taking the positional deviation of the U-groove with respect to the base layer end into account as in the conventional U-MOS, but the length of the bottom face of the U-groove can be made short into the necessary minimum. As a result, the unit cell size can be greatly reduced, the ON-resistance per area can be reduced into a degree equivalent to the R-MOS, and the production yield and the reliability are high in a degree equivalent to the DMOS type, so that it is extremely effective in adoption as switching devices for electric power and the like as MOSIC in which its elemental article or the device is incorporated.

Claims

1. A production method of a vertical type MOSFET characterized in that it comprises

a local oxidation step which includes a step of preparing a semiconductor substrate, a step of forming a semiconductor layer of the first conductive type at one main face side of said semiconductor substrate, where said semiconductor layer has an impurity concentration lower than that of the semiconductor substrate and the surface of said semiconductor layer of the low concentration is used as a main surface, and a step of local oxidizing a predetermined region of said main surface, thereby a local oxide film having a predetermined depth from said main surface is formed in said semiconductor

layer in the predetermined region,

an impurity introduction step in which in order to form channels on said semiconductor layer surface contacting with a side face of said local oxide film, impurities of the second conductive type and the first conductive type are doubly diffused from said main surface successively in a manner of self-alignment with respect to said local oxide film, and the length of said channel is determined by the double diffusion, simultaneously with which a base layer of the second conductive type and a source layer of the first conductive type are formed,

a gate formation step in which said local oxide film is removed after the double diffusion to form a groove structure having said predetermined depth, an inner wall of said groove including a portion to become said channel is oxidized to provide a gate oxide film, and a gate electrode is formed on the gate oxide film, and

a source and drain electrodes formation step in which a source electrode which electrically contacts with both said source layer and said base layer, and a drain electrode which electrically contacts with the other main face side of said semiconductor substrate are formed.

2. The production method of the vertical type MOSFET according to claim 1 characterized in that it is provided with a condition setting step in which a condition is selected such that a film thickness of said gate oxide film is thicker at a bottom face portion of said groove than a thickness of the gate oxide film at a side face portion of said groove during the formation of the gate oxide film in said gate formation step.

3. The production method of the vertical type MOSFET according to claim 2 characterized in that said condition setting step is a index of plane selection step in which a index of plane of the semiconductor crystal surface at the bottom face portion of said groove, and a index of plane of the semiconductor crystal surface at the side face portion of said groove are selected.

4. The production method of the vertical type MOSFET according to claim 3 characterized in that said index of plane selection step is a step in which in said local oxidation step, said semiconductor layer is silicon, a index of plane of said main surface thereof is (1 1 1) or a face near (1 1 1), and a index of plane of said semiconductor layer surface contacting with the side face of said selected oxide film is (1 0 0) or a face near (1 0 0).

5. The production method of the vertical type MOSFET according to claim 1 characterized in that during the gate oxide film formation in said gate formation step, an oxidation velocity of the inner wall of said groove is selected to be a reaction controlled oxidation condition.

6. The production method of the vertical type MOSFET according to claim 3 characterized in that during the gate oxide film formation in said gate formation step, an oxidation velocity of the inner wall of said groove is selected to be a reaction contolled oxidation condition.

7. The production method of the vertical type MOSFET according to claim 4 characterized in that during the gate oxide film formation in said gate formation step, an oxidation velocity of the inner wall of said groove is selected to be a reaction controlled oxidation condition.

8. The production method of the vertical type MOSFET according to claim 1 characterized in that said semiconductor substrate is the first conductive type.

9. The production method of the vertical type MOSFET according to claim 1 characterized in that said semiconductor substrate is the second conductive type.

10. The production method of the vertical type MOSFET according to claim 1 characterized in that said local oxidation step includes initial groove formation in which the main surface is etched to give a predetermined depth in the region for forming the local oxide film on the main surface of said semiconductor layer prior to the formation of said local oxide film.

11. The production method of the vertical type MOSFET according to claim 3 characterized in that said local oxidation step includes initial groove formation in which the main surface is etched to give a predetermined depth in the region for forming the local oxide film on the main surface of said

semiconductor layer prior to the formation of said local oxide film.

12. The production method of the vertical type MOSFET according to claim 4 characterized in that said local oxidation step includes initial groove formation in which the main surface is etched to give a predetermined depth in the region for forming the local oxide film on the main surface of said semiconductor layer prior to the formation of said local oxide film.

13. The production method of the vertical type MOSFET according to claim 4 characterized in that in said local oxidation step, the surface pattern shape of said local oxide film is an equilateral triangle, the direction of one side thereof is set in the index of plane ⟨2 1 1⟩.

14. The production method of the vertical type MOSFET according to claim 1 characterized in that an inclination angle of the side face of said selected oxide film with respect to the main surface of said semiconductor layer is set to be not less than 45°.

15. The production method of the vertical type MOSFET according to claim 1 characterized in that an inclination angle of the side face of said local oxide film with respect to the main surface of said semiconductor layer is set to be an angle with which an interface state density of said semiconductor layer surface contacting to the side face becomes low.

16. The production method of the vertical type MOSFET according to claim 7 characterized in that an inclination angle of the side face of said local oxide film with respect to the main surface of said semiconductor layer is set to be an angle with which an interface state density of said semiconductor layer surface contacting to the side face becomes low.

FIG.1(a)

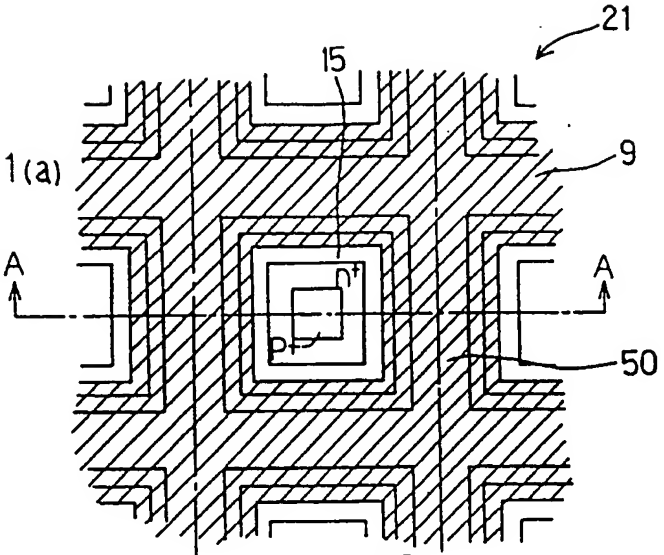


FIG.1(b)

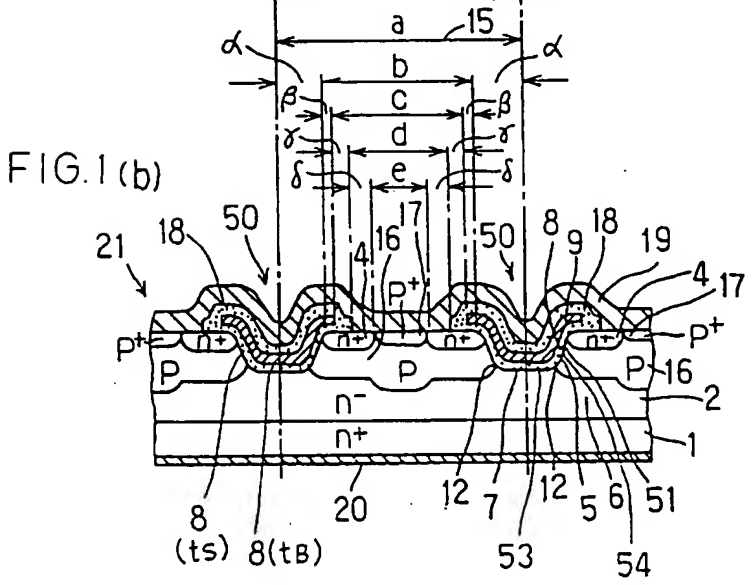


FIG.2

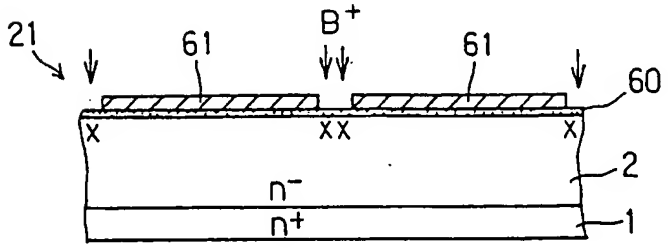


FIG.3

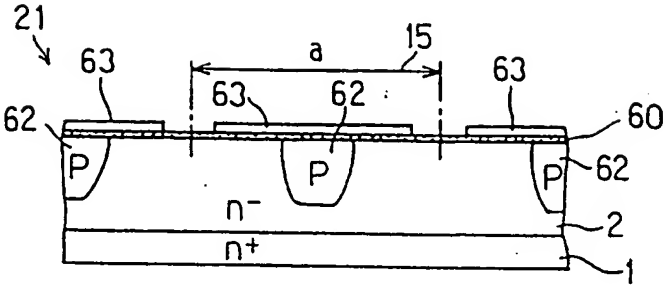


FIG.4

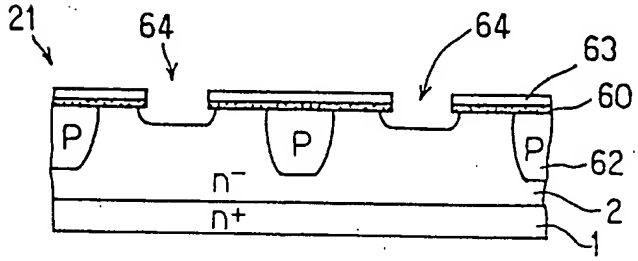


FIG.5

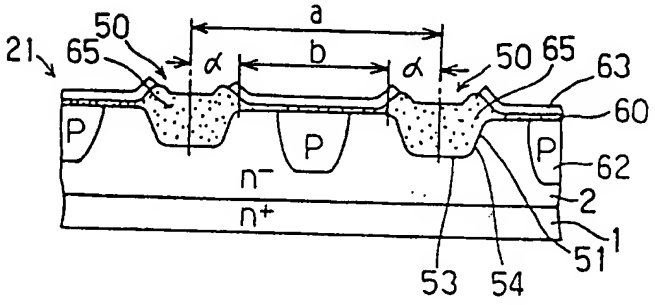


FIG.6

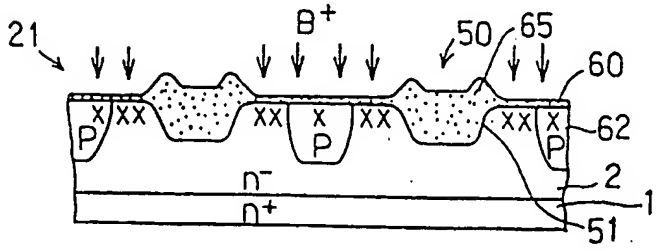


FIG.7

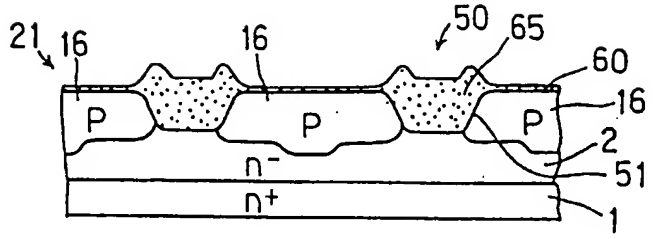


FIG.8

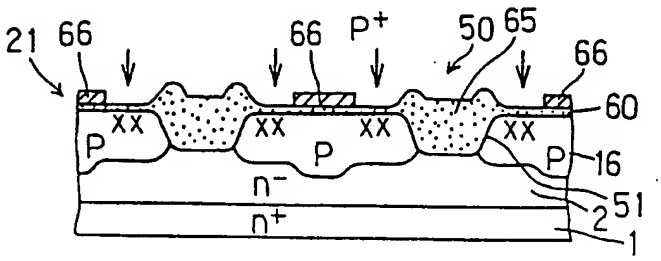


FIG.9

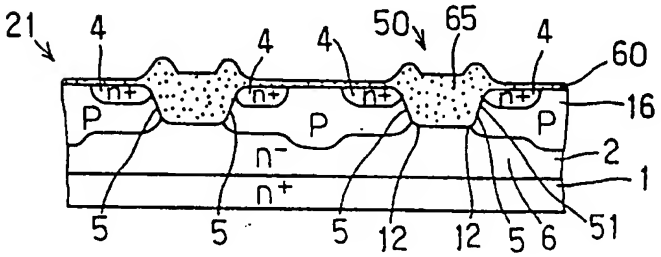


FIG.10

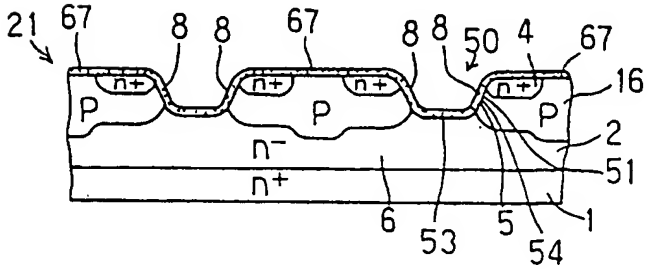


FIG.11

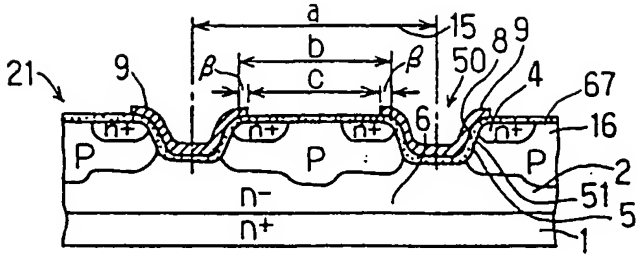


FIG.12

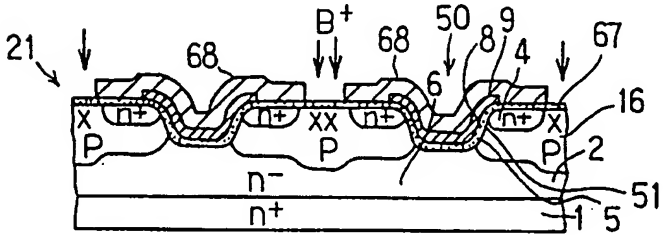


FIG.13

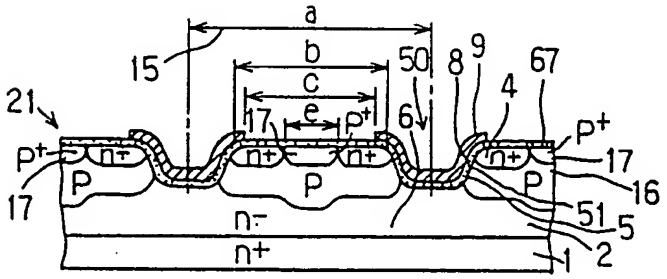


FIG.14

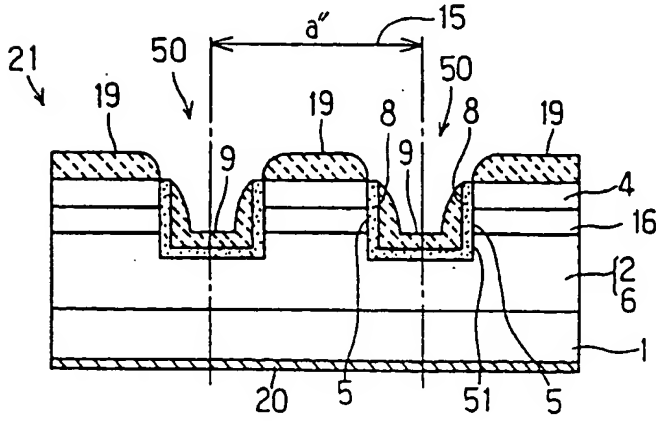


FIG.15

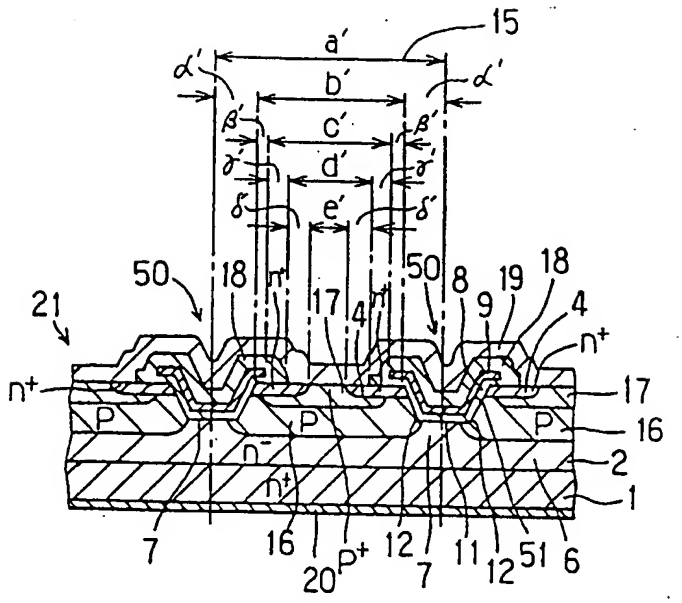


FIG.16

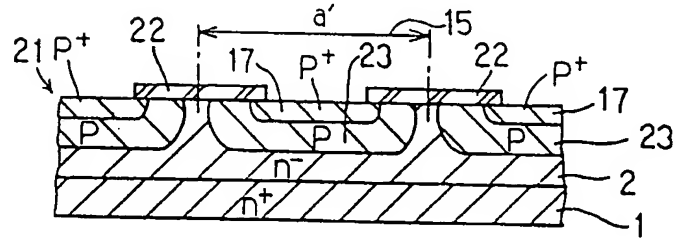


FIG.17

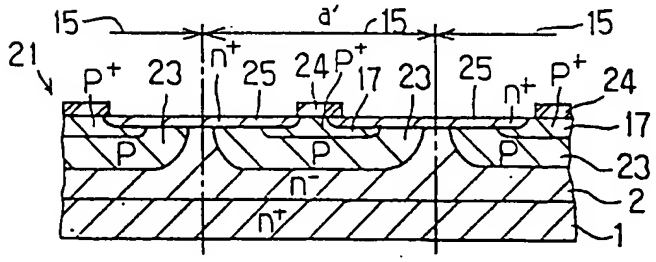


FIG. 18

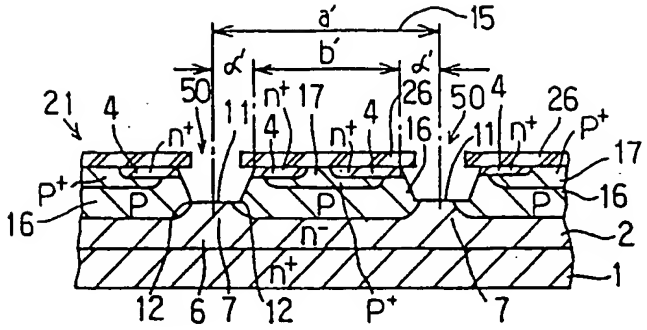


FIG. 19

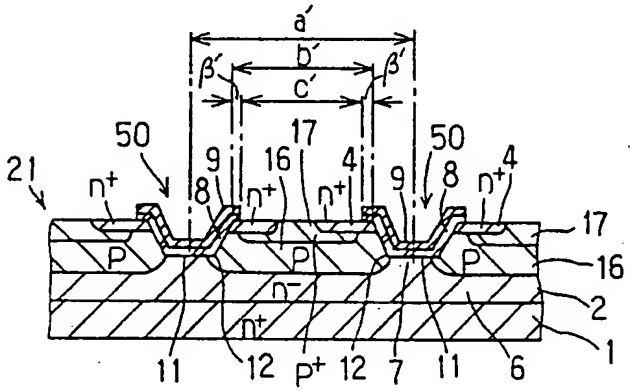


FIG. 20

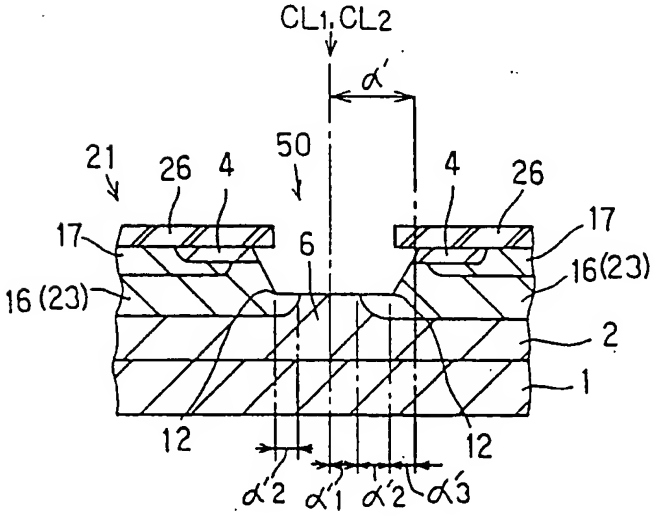


FIG. 21

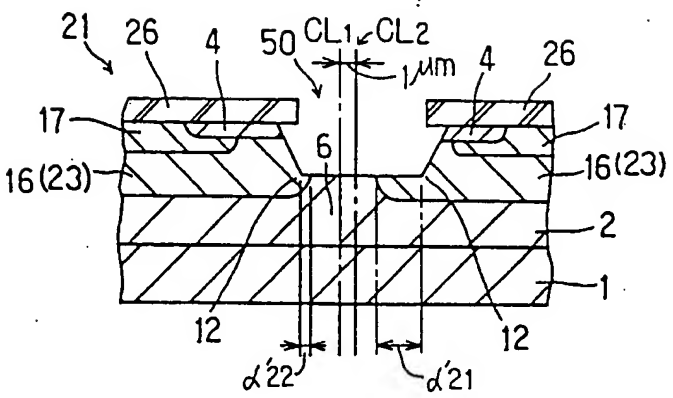

21
26
4
50
CL1
CL2
1μm
4
26
17
17
6
16(23)
16(23)
2
1
12
12
α'22
α'21

FIG. 22

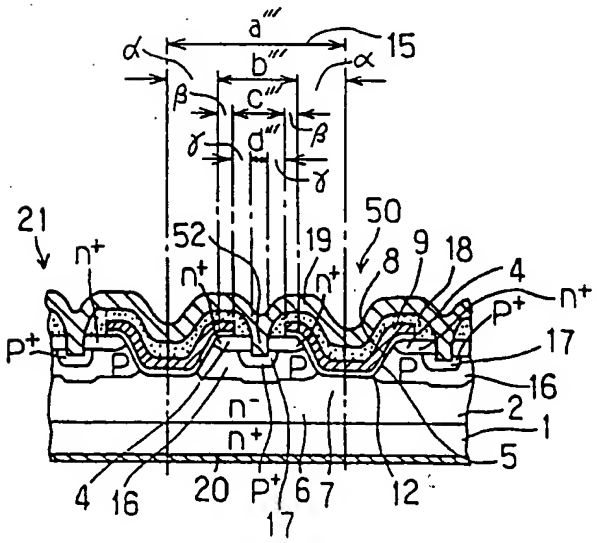

a'''
α
15
α
b'''
β
c'''
β
γ
d'''
γ
21
50
52
19
9
18
n+
n+
n+
8
4
n+
P+
P+
17
P
P
P
16
n-
2
n+
1
5
4
16
20
P+
6
7
12
17

FIG.23 (a)

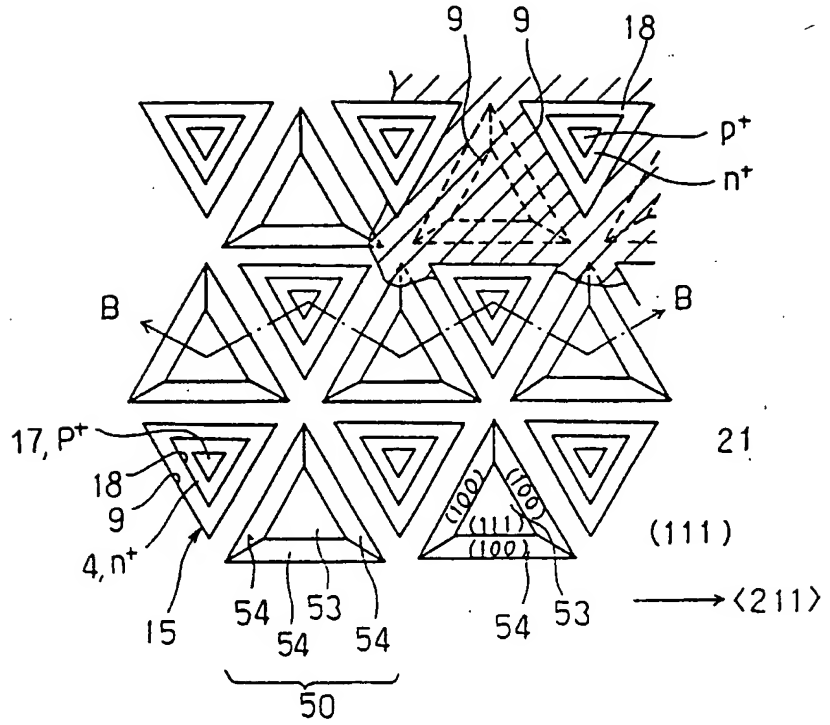
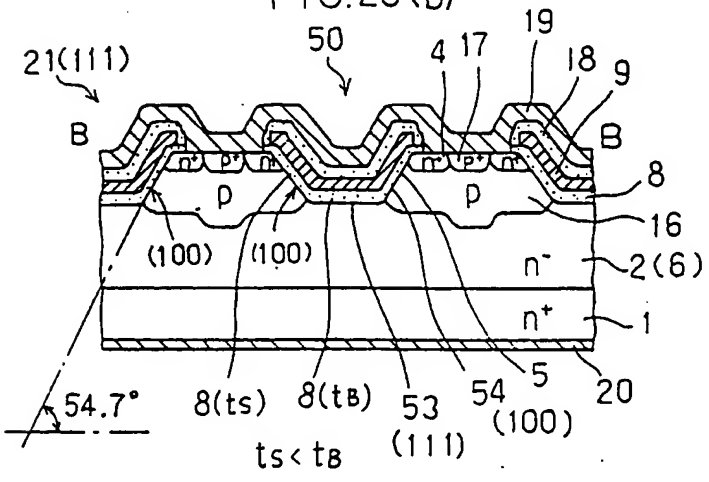


FIG.23 (b)



INTERNATIONAL SEARCH REPORT

International Application No PCT/JP92/00929

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl[5] H01L29/784

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC	H01L29/784

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [8]

Jitsuyo Shinan Koho 1926 - 1991
Kokai Jitsuyo Shinan Koho 1971 - 1991

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	JP, A, 62-12167 (TDK Corp.), January 21, 1987 (21. 01. 87), (Family: none)	1, 8, 9, 10, 14
X	JP, A, 60-28271 (Nissan Motor Co., Ltd.), February 13, 1985 (13. 02. 85), & DE, A1, 3427293	1, 8
Y	JP, A, 62-46569 (TDK Corp.), February 28, 1987 (28. 02. 87), (Family: none)	1, 2, 8
Y	JP, A, 54-91187 (Techtoronics, Inc.), July 19, 1979 (19. 07. 79), & CA, A1, 1119733 & DE, A1, 2854073 & FR, A1, 2412942 & GB, A, 2011170 & GB, B, 2011170 & JP, B2, 63-18346 & NL, A, 7811920 & US, A, 4217599 & US, A, 4261761	1, 5
Y	JP, A, 56-96865 (Fujitsu Ltd.), August 5, 1981 (05. 08. 81), (Family: none)	1, 10

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
October 20, 1992 (20. 10. 92)	November 2, 1992 (02. 11. 92)
International Searching Authority	**Signature of Authorized Officer**
Japanese Patent Office	

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

Y	JP, A, 1-192174 (Hitachi, Ltd.), August 2, 1989 (02. 08. 89), (Family: none)	2
Y	JP, A, 56-150870 (RCA Corp.), November 21, 1981 (21. 11. 81), & DE, A1, 3110230 & FR, A1, 2479567 & FR, B1, 2479567 & GB, A, 2072422 & GB, B, 2072422 & IT, A, 1194027 & IT, AO, 8120225 & JP, B2, 61-50397 & PL, A1, 230318 & PL, B1, 137347 & SE, A, 8101263 & SE, B, 456292 & SE, C, 456292 & US, A, 4364073 & YU, A, 77481 & YU, B, 43009	9

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [1]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers . . . , because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claim numbers . . . , because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claim numbers . . . . , because they are dependent claims and are not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [2]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

A	JP, A, 54-146584 (Mitsubishi Electric Corp.), November 15, 1979 (15. 11. 79), (Family: none)	1, 14
A	JP, A, 63-266882 (Hitachi, Ltd.), November 2, 1988 (02. 11. 88), (Family: none)	1
A	JP, A, 2-86136 (Hitachi, Ltd.), March 27, 1990 (27. 03. 90), (Family: none)	1
A	JP, A, 2-86171 (Hitachi, Ltd.), March 27, 1990 (27. 03. 90), (Family: none)	1

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [1]

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3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

A	JP, A, 59-8374 (Matsushita Electronics Corp.), January 17, 1984 (17. 01. 84), (Family: none)	1
A	JP, A, 53-16581 (Toshiba Corp.), February 15, 1978 (15. 02. 78), & DE, A1, 2724165	1
A	JP, A, 58-166759 (NEC Corp.), October 1, 1983 (01. 10. 83), (Family: none)	2-4, 15
A	JP, A, 2-262375 (Toshiba Corp.), October 25, 1990 (25. 10. 90),	2-4

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [1]

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Remark on Protest

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☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

	(Family: none)	
A	JP, A, 1-189172 (Sharp Corp.), July 28, 1989 (28. 07. 89), (Family: none)	2-4
A	Journal of Electrochemical Society:Solid-State Science and Technology, Vol. 124, No. 2 (February, 1977), H. Sakai et al.: "Methods to Improve the Surface Planarity of Locally Oxidized Silicon Devices", pp. 318-320	10, 14
A	JP, A, 59-8375 (Matsushita Electronics Corp.),	13-15

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [1]

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1. ☐ Claim numbers . . , because they relate to subject matter not required to be searched by this Authority, namely:

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3. ☐ Claim numbers . . . . . , because they are dependent claims and are not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

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3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

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Remark on Protest

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☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

	January 17, 1984 (17. 01. 84), & DE, A1, 3324017 & DE, C3, 3324017	
A	IEEE Transactions on Electron Devices, Vol. ED-32, No. 1 (January, 1985), (New York), D. Ueda et al.: "A New Vertical Power MOSFET Structure with Extremely Reduced On-Resistance", pp. 2-6	13-15

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [1]

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This International Searching Authority found multiple inventions in this international application as follows:

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2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

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4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

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